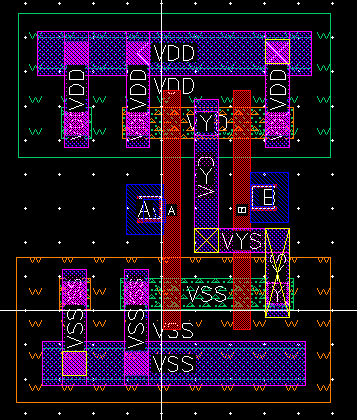
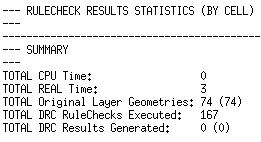
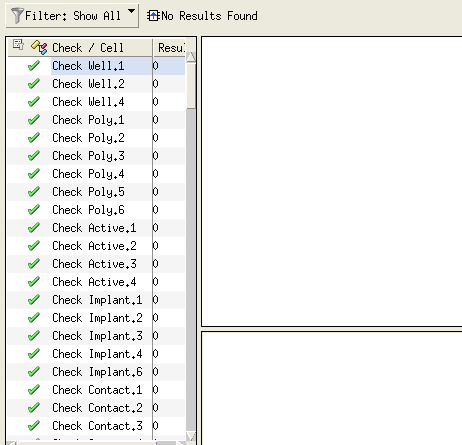
**1) NAND gate:**

Layout:

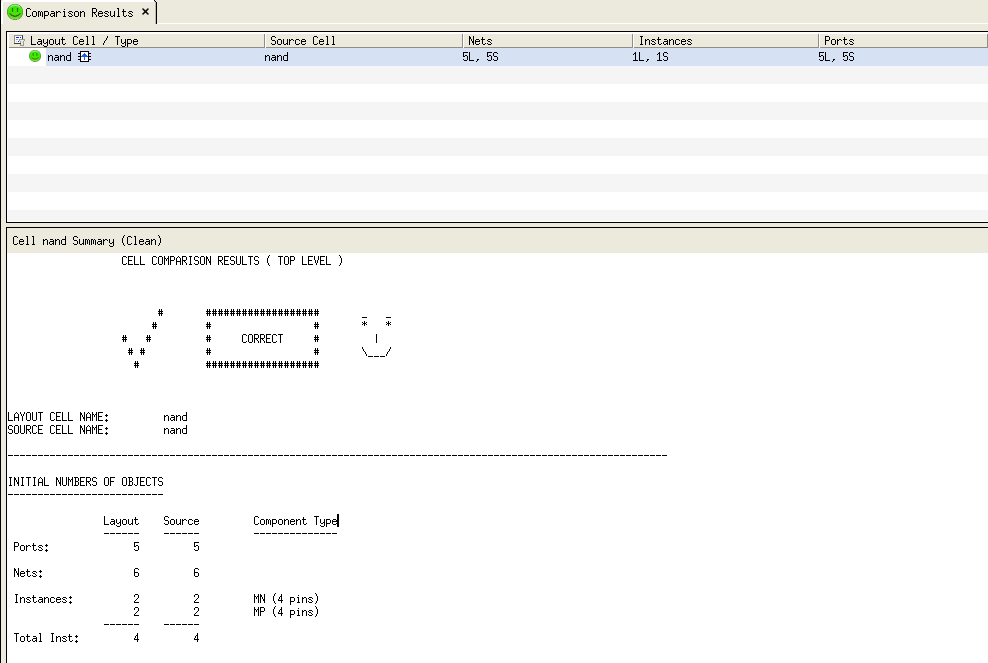


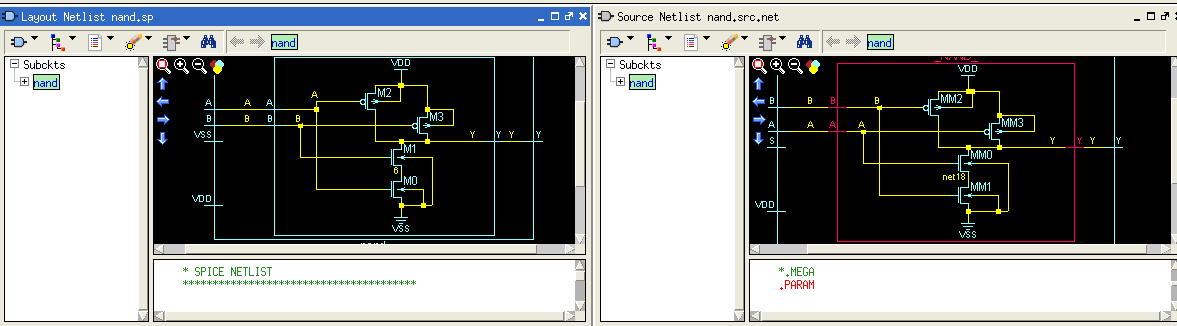
Check DRC:





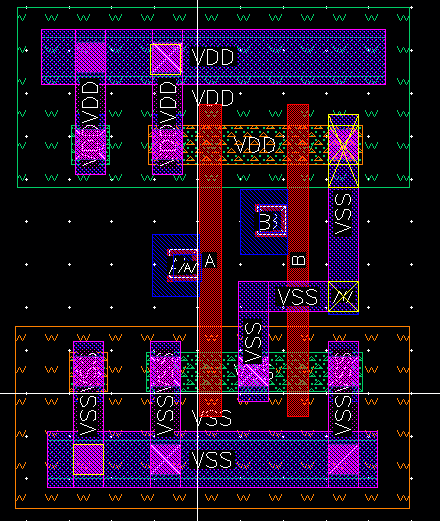
Check LVS:



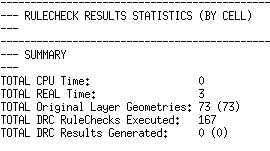


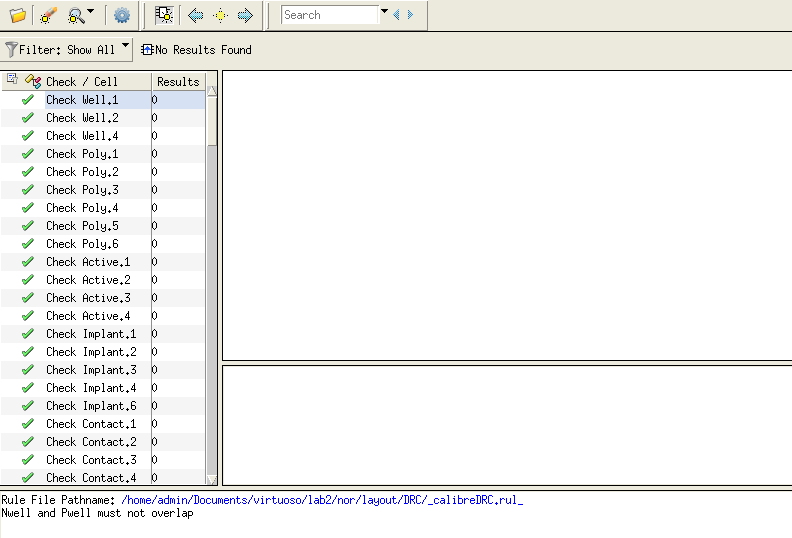
**2) NOR gate:**

Layout:

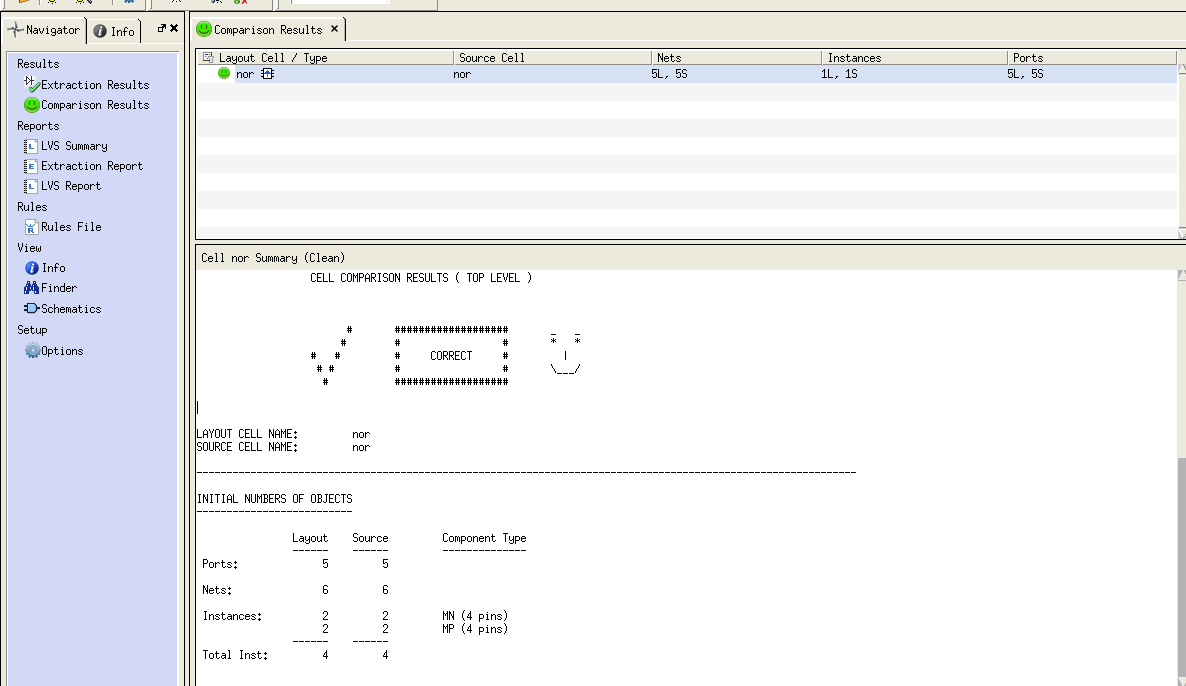


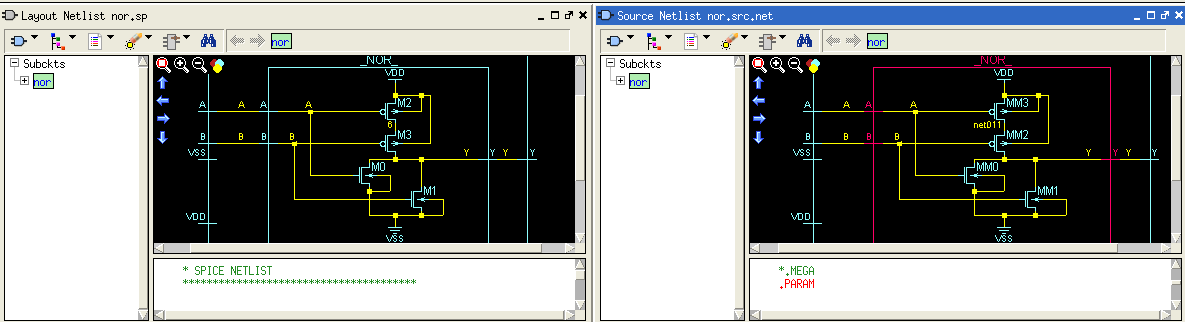
Check DRC:





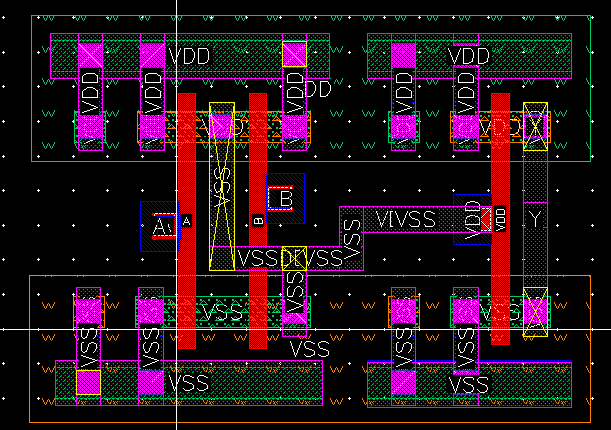
Check LVS:



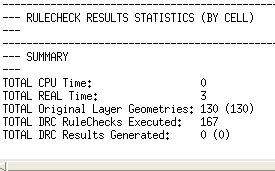


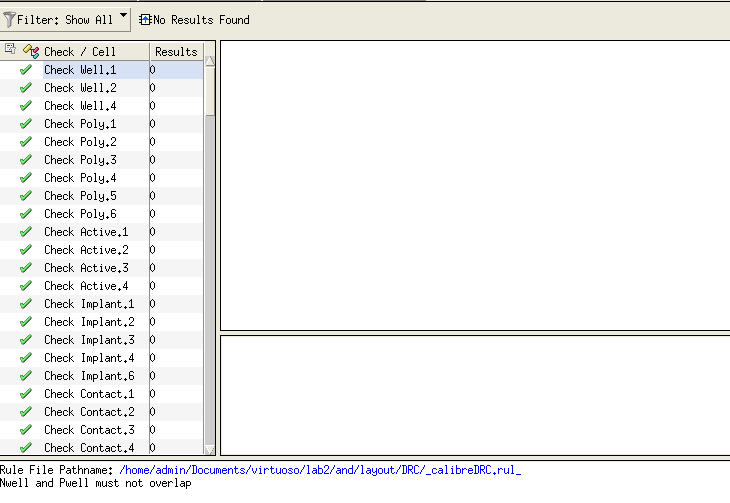
**3) AND gate:**

Layout:



Check DRC:





Check LVS:

